REMARKS

Applicants have amended the title of the above-identified application to properly reflect the subject matter being claimed therein. In view of this new title, it is respectfully submitted that the requirement for a new title as set forth in Item 1 on page 2 of the Office Action mailed September 9, 2004, has been satisfied.

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants are amending previously considered claims 1-28 to avoid formal issues in connection therewith, and are adding new claims 29-34 to the application. Specifically, claim 25 has been amended to recite the second principal "plane"; and claim 28 has been amended to provide "and" between the next-to-last and last steps only (deleting "and:" between steps (c) and (d), and to recite in step (g) a third single wafer processing "unit". Of the new claims, claims 29 and 30, dependent respectively on claims 1 and 29, respectively recites that the protective film is a silicon oxide film, and recites that this silicon oxide film is formed by a CVD method. Note, for example, previously considered claims 26 and 27. Claims 33 and 34, dependent respectively on claims 28 and 33, respectively recites that the insulating film is formed by a CVD method, and that the insulating film includes an oxide film formed by the CVD method. Again, note previously considered claims 26 and 27. Claims 31 and 32, dependent respectively on claims 18 and 1, respectively recites that the cleaning is performed using a fluorine-containing cleaning solution, and recites that the protective film has a thickness of 20 to 500 nm. In connection with claims 31 and 32, note, for example, pages 22 and 23 of Applicants'

specification.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed September 9, 2004, that is, the teachings of the U.S. patents to Kraft, et al., No. 6,136,654, to Maydan, et al., No. 5,882,165, to Hayashi, et al., No. 6,780,278, to Denning, et al., No. 6,187,682, to Shih, et al., No. 6,589,852, to Kawakubo, No. 6,242,398, and to Beauchaine, et al., No. 6,576,501, United States Patent Application Publication No. US 2003/0173601 to Machida, et al., and Wolf, et al., Silicon Processing For The VLSI Era (Volume 1: Process Technology), page 198, under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a manufacturing method of a semiconductor device, as in the present claims, including, inter alia, preparation of a semiconductor wafer having the specified planes as in the present claims, and forming a protective film on the second principal plane (only - see claim 1) of the semiconductor wafer (see claims 1, 10 and 18), and wherein a gate insulating film is formed on the first principal plane after forming this protective film (see claim 1); or wherein a gate insulating film is formed on the first principal plane and a conductive film is formed on the gate insulating film, with the protective film being formed after forming the conductive film, the protective film being formed with the first principal plane of the semiconductor wafer placed on a support in a first apparatus (see claim 10); or wherein

the protective film is formed with the first principal plane of the semiconductor wafer placed on a support in a first apparatus, a metal or a metallic compound being formed on the first principal plane after forming the protective film, and wherein the second principal plane of the semiconductor wafer is cleaned after forming the metal or metallic compound on the first principal plane (see claim 18).

Furthermore, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a manufacturing method of a semiconductor device as in the present claims, including preparation of a semiconductor wafer having the recited first and second principal planes and having a diameter of about 300 mm or not smaller than 300 nm, and allowing a film to be formed so as to cover the second principal plane of the semiconductor wafer (see claims 21 and 28); and, moreover, wherein the semiconductor wafer is mounted on a susceptor in a single wafer processing unit so that the film on the second principal plane comes in contact with the susceptor, and the first principal plane of the wafer is processed by the single wafer processing unit (see claim 21; note also claim 28); and, in particular, wherein after mounting the semiconductor wafer on the susceptor a gate insulating film is formed on the first principal plane within the first single wafer processing unit, the semiconductor having the gate insulating film thereon is mounted on a susceptor in a second single wafer processing unit so that the insulating film on the second principal plane comes in contact with the susceptor, and a metal or a semiconductor is formed on the gate insulating film within the second single wafer processing unit, the semiconductor wafer having the metal or semiconductor thereon is mounted on a

susceptor in a third single wafer processing unit so that the insulating film on the second principal plane comes in contact with the susceptor and the metal or semiconductor within the third single wafer processing unit is selectively etched to form a gate electrode, and in a fourth single wafer processing unit the semiconductor wafer is cleaned (see claim 28).

In addition, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a manufacturing method of a semiconductor device as in the present claims, having features as discussed previously in connection with each of the independent claims 1, 10, 18, 21 and 28, and further including (but not limited to) wherein the protective film is a (silicon) oxide film, formed by a CVD method (note, for example, but not limited to, claims 26, 27, 29 and 30); and/or the mounting of the semiconductor on a support and forming a conductive film, with the conductive film being etched into a predetermined pattern (see claim 3), the etching being performed under a plasma atmosphere (see claim 4); and/or wherein the wafer is cleaned after forming the protective film (see claim 5); and/or forming trenches for element isolation after formation of the protective film and before forming the gate insulating film (see claim 6), or prior to forming the protective film (see claims 7 and 14); and/or wherein the wafers processed have a diameter of about 300 mm, or not smaller than 300 mm (see, e.g., claims 8 and 16; note also claims 21 and 28); and/or the step of cleaning the semiconductor wafer, after forming the gate insulating film (see claim 13); and/or wherein the gate insulating film is formed by thermal oxidation and then oxynitride processing (see claim 15); and/or

wherein the metal or metallic compound formed on the first principal plane is a copper film (see claim 19), particularly formed by plating (see claim 20); and/or wherein the cleaning is performed using a fluorine-containing cleaning solution (see claim 31), and/or wherein the protective film has a thickness of 20-500 nm (see claim 32).

The present invention is directed to a manufacturing method of semiconductor devices, particularly suitable for treatment of large-diameter semiconductor wafers (for example, 300 mm or greater), which are processed by single wafer processing units.

In the manufacturing process of semiconductor devices in which emphasis is placed on uniformity and controllability of processing, a so-called single wafer processing is performed in which processing is performed for a unit of one semiconductor wafer. In the semiconductor wafer used for manufacturing the semiconductor device, a face (back side), or second plane, opposite to a face (surface) or first plane on which an element is formed, may be processed. Various techniques for processing the back side of the wafer are described, on pages 2 and 3 of Applicants' specification. However, in these techniques described on pages 2 and 3 of Applicants' specification, problems arising in connection with the single wafer processing have not been disclosed. In particular, Applicants have found that, in such single wafer processing, and particularly when processing large-diameter semiconductor wafers, various problems such as contamination on the back side of the semiconductor wafer, and deterioration in resisting pressure of a gate insulating film of an MISFET formed on such wafer occur, as described from page 5, line 16 through page 6, line 18, of Applicants' specification. In particular, these problems include adherence of

contaminant particles to the back side (of Si) of the semiconductor wafer, since this back side is hydrophobic, which contaminant materials become a contamination source on the wafer surface on which elements are formed; and the gate insulating film may be broken due to electric charge accumulated on the semiconductor wafer during the manufacturing process.

Against this background, Applicants provide a method avoiding problems arising in connection with prior art processing; and, in particular, which avoids contamination problems and breaking of the gate insulating film due to accumulated electric charge. Applicants have found that by forming a protective film on the second principal plane of the semiconductor wafer (that is, on the back side thereof), such problems in connection with prior art techniques can be avoided. Specifically, through use of a protective film (e.g., a silicon oxide film) on the back side, contaminants are less likely to adhere thereto, and can more easily be removed by cleaning. In particular, by cleaning using a fluorine-containing cleaning solution, a surface part of the protective film can be stripped off, whereby any adhering contaminants are lifted off from the protective film.

Furthermore, when forming the protective film on the back side of the semiconductor substrate, the gate insulating film and the protective film are connected in series between the conductive film, being a gate electrode, and the semiconductor substrate, and hence influence of the electric charge with respect to the gate insulating film can be lowered (that is, a voltage applied to the gate insulating film is reduced). Note, for example, from page 21, line 14 through page 23, line 6, of Applicants'

specification. See also page 37, lines 19-26; and page 50, line 15 through page 51, line 1, of Applicants' specification.

Machida, et al. discloses a functional device having a functional layer, such as a thin film transistor, a dielectric capacitor, or a solar battery, and a method of manufacturing the same. See paragraph [0001] on page 1 of this patent document. The method includes forming a low-temperature softening layer having a softening temperature lower than that of a substrate on the substrate; forming a heat-resistant layer which is a single layer or constructed by a plurality of layers on the low-temperature softening layer; and forming the functional layer on the heat-resistant layer. See paragraph [0009]. This patent document further discloses that it is preferable to provide a warp suppression layer for suppressing a warp which occurs in association with thermal deformation of the substrate on the surface opposite to the surface of the substrate upon which the functional layer is provided. See paragraph [0012]. Note also paragraphs [0010], [0030], [0031] and [0036]. Note further paragraphs [0039], [0067] and [0069]. This patent document further discloses, in paragraph [0114] on page 8, that with respect to the functional device comprising the substrate 11 (note Fig. 1), the substrate 11 may be removed after fabricating the functional device, or the invention can be applied to a functional device which does not comprise the substrate 11.

It is emphasized that Machida, et al. discloses a device including a functional layer. It is respectfully submitted that this reference does not disclose, nor would have suggested, such method as in the present claims, including preparation and processing

of a semiconductor wafer, problems arising in connection therewith and avoidance of such problems through use of the protective film on the back surface of the semiconductor wafer, as in the present claims.

The contention by the Examiner in the last paragraph on page 2 of the Office Action mailed September 9, 2004, that Machida, et al. discloses preparing a semiconductor wafer 11, is respectfully traversed. It is respectfully submitted that the structure represented by reference character 11 in Machida, et al. is a substrate, not a semiconductor wafer. It is respectfully submitted that the semiconductor in Machida, et al. is a semiconductor layer 14. Noting that Machida, et al. indicates that the invention is directed to a functional device having a functional layer (note paragraph [0001] thereof), it is respectfully submitted that this reference would have taught away from processing of a semiconductor wafer, and problems arising in connection therewith, and especially in connection with single wafer processing, as in various aspects of the present invention.

As will be shown in the following, it is respectfully submitted that the secondary references as applied by the Examiner would not have rectified the deficiencies of Machida, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Wolf, et al., as applied by the Examiner, discloses formation of silicon oxide on a silicon surface, e.g., by thermal oxidation in which the silicon is exposed to an oxidizing ambient at elevated temperatures. See page 198 of Wolf, et al.

Even assuming, arguendo, that the teachings of Wolf, et al. were properly

combinable with the teachings of Machida, et al., such combined teachings would have neither disclosed nor would have suggested the processing of semiconductor wafers, as in the present invention.

Kraft, et al. discloses a method of forming a transistor having a conductive gate structure disposed on a gate dielectric layer, wherein the dielectric layer is subjected to a nitrogen containing plasma so that nitrogen is either incorporated into the gate insulating layer or forms a nitride layer at the surface of the substrate. See column 2, lines 53-64.

Even assuming, arguendo, that the teachings of Kraft, et al. were properly combinable with the teachings of Machida, et al. and Wolf, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed invention, including, inter alia, processing of the semiconductor wafers, with forming of the protective film on the second plane of the semiconductor wafer, and advantages thereof as discussed previously.

Maydan, et al. discloses an integrated vacuum process system which includes a vacuum load lock chamber having at least one and preferably a plurality or multiplicity of vacuum processing chambers mounted to the exterior thereof, each of the processing chambers being adapted to perform one or more processes selected from, for example, gas chemistry etching, gas chemistry deposition, physical sputtering and rapid thermal anneal of one or more wafers positioned within the chamber. See column 2, lines 38-53.

It is respectfully submitted that one of ordinary skill in the art concerned with in

Machida, et al., directed to thin film devices, would not have looked to the teachings of Maydan, et al., treating wafers.

In any event, even assuming, arguendo, that the teachings of Maydan, et al., as applied by the Examiner, were properly combinable with the teachings of Machida, et al., it is respectfully submitted that the teachings of these references would have neither disclosed nor would have suggested allowing formation of the film on the second plane of the semiconductor wafer, as in the present claims, and advantages thereof; and/or the other features of the present invention as in claims 3, 21 and 28, and discussed previously, and advantages thereof.

Hayashi, et al. discloses a plasma processing apparatus for producing plasma under application of a radio frequency (RF) and for carrying out etching or CVD processes. This patent discloses that a parallel plate type plasma etching apparatus is generally used in semiconductor manufacturing processes; and goes on to disclose a plasma processing apparatus which includes a grounded housing, a thin RF plate electrode placed in the housing, an opposite electrode facing the RF plate electrode and an RF power source, which can reduce a loss of RF power even at high radio frequencies. See column 1, lines 13-18; and column 2, line 58 through column 3, line 2.

Even assuming, arguendo, that the teachings of Hayashi, et al., as applied by the Examiner, were properly combinable with the teachings of Machida, et al., such combined teachings would have neither disclosed nor would have suggested the formation of the protective film on the second plane of the semiconductor wafer, and

advantages thereof; and/or the other features of the present invention as discussed previously, and advantages thereof.

Denning, et al. discloses performance of an in situ argon plasma clean on a surface of a substrate just prior to sputtering a surface-critical film on the surface of the substrate. See column 1, lines 7-11. As for the disclosed method, note from column 2, line 66 to column 3, line 12. This patent discloses that biasing the wafer directs charged ions from the plasma down towards the wafer surface to result in physical sputtering of contaminants and oxides from a surface of the wafer, the sputtering off the wafer surface results in cleaning of the wafer surface. Note also column 3, lines 13-20.

Even assuming, arguendo, that the teachings of Denning, et al. as applied by the Examiner were properly combinable with the teachings of Machida, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed invention, including providing the protective film on the second plane of the semiconductor wafer, and/or cleaning of the manufactured structure, particularly the protective film. It is emphasized that according to the present invention, by cleaning of the protective film, various contaminants disadvantageously provided on the second plane of the semiconductor wafer can be removed, e.g., by stripping off a top portion of the protective film. Clearly, the combined teachings of Machida, et al. and Denning, et al. would have neither taught nor would have suggested this feature of the present invention.

The contention by the Examiner on page 6 of the Office Action mailed September 9, 2004, that it would have been obvious to clean the surface in

Machida, et al., to obtain atomically or near atomically clean substrate surfaces prior to formation of various films over the top of these surfaces, is noted. It is respectfully submitted, however, that the cleaning according to the present invention can, e.g., remove contaminants from the second plane of the semiconductor wafer. It is respectfully submitted that the teachings of Denning, et al. would have neither taught nor would have suggested this feature of the present invention.

Shih, et al. discloses semiconductor processing methods including photolithographic patterning, and describes that shallow trench isolation is a preferred electrical isolation technique especially for a semiconductor chip with high integration. See column 1, lines 7-10 and 30-32. This patent is primarily directed to providing alignment mark areas, as described in column 3, lines 24-38 of this patent.

It is again emphasized that Machida, et al. is directed to thin film devices. In view thereof, it is respectfully submitted that one of ordinary skill in the art would not have looked to the teachings of Shih, et al., as applied by the Examiner, disclosing shallow trench isolation.

In any event, even assuming, arguendo, that the teachings of Shih, et al. were properly combinable with the teachings of Machida, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including formation of the protective film on the second plane of the semiconductor wafer, much less the sequencing of processing steps including forming the trenches and forming the protective film, as in the present claims.

Kawakubo discloses a semiconductor memory device having an ultrahigh density

of integration above 1 gigabit, using an epitaxial planar capacitor possessing a dielectric thin film made of dielectric material having a perovskite-type structure or another crystal structure, and methods of making such device, a method of fabricating such device being described, for example, in column 7, lines 38-51. See also column 7, lines 5-10. Note further a third feature of the device described in Kawakubo, at column 9, lines 21-35; and the description that according to this third feature, it is possible to use a silicon wafer (semiconductor substrate) with a diameter greater than 200 mm (8 inches) to 300 nm (12 inches).

Initially, it is respectfully submitted that the teachings of Machida, et al. are not properly combinable with the teachings of Kawakubo as applied by the Examiner. Thus, Kawakubo discloses treatment of semiconductor wafers; <u>in contrast</u>, Machida, et al. discloses use of functional <u>layers</u> (for example, <u>thin film</u> semiconductor devices). It is respectfully submitted that one of ordinary skill in the art concerned with in Machida, et al., directed to use of functional <u>layers</u>, would not have looked to the semiconductor <u>wafers</u> of Kawakubo.

In any event, even assuming, <u>arguendo</u>, that the teachings of these applied references were properly combinable, it is respectfully submitted that such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including forming of the protective film, or allowing the film to be formed, on the <u>second plane of the semiconductor wafer</u>, and advantages thereof; and/or other features of the present invention as discussed in the foregoing, and advantages thereof, including use of the single wafer processing apparatus.

Beauchaine, et al. discloses a method of processing double side polished wafers that contain external gettering sites, wherein a semiconductor substrate wafer is prepared by slicing an ingot into wafers; a wafer is then subjected to an edge grinding process, where the periphery of the wafer is chamfered to increase strength and remove sharp edges that can easily be chipped or broken; both surfaces of the wafer are lapped or subjected to surface grinding to remove slicing damage and to make the front and back surfaces both flat and parallel to each other; after lapping or surface grinding, the wafer is chemically etched; and the back side of the wafer is then polished to a complete, or mirror polish. See column 2, lines 36-67. This patent goes on to disclose that after the back side of the wafer is polished, a thin polysilicon layer is deposited on the wafer, and the wafer is then subjected to an oxidation step. The oxidation step consumes the polysilicon layer and forms stacking faults at the back surface of the wafer. Once the stacking faults are formed, the oxide layer is then stripped from both sides of the wafer, and the front side of the wafer is subjected to a complete polish. See column 3, lines 1-8. Note also column 3, lines 45-49 and 56-65; and column 4, lines 4-6, 12 and 13.

As discussed previously, and noting that Beauchaine, et al. is concerned with a manufacturing process of a semiconductor wafer while Machida, et al. is directed to fabrication of functional devices using functional layers, it is respectfully submitted that one of ordinary skill in the art concerned with in Machida, et al. would not have looked to the teachings of Beauchaine, et al.

In any event, even assuming, arguendo, that the teachings of Machida, et al. and

of Beauchaine, et al., as applied by the Examiner, were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including the protective film formed on the back surface of the semiconductor wafer, and advantages thereof; and/or the other features of the present invention as discussed previously, and advantages thereof.

In Items 14, 18 and 19, the Examiner has respectively applied the combined teachings of Machida, et al. and Denning, et al.; Machida, et al., Denning, et al. and Shih, et al.; and Machida, et al., Denning, et al. and Beauchaine, et al. As discussed previously, it is respectfully submitted that the teachings of various of these references, such as Machida, et al. and Beauchaine, et al., and/or Denning, et al. would not have been properly combinable.

However, even if the teachings of these references as applied in Items 14, 18 and 19 were properly combinable, such combined teachings as applied by the Examiner would have neither disclosed nor would have suggested the presently claimed subject matter, including forming of the protective film and/or allowing the, e.g., insulating film to be formed, on the second plane of the semiconductor wafer, and advantages thereof; and/or use of the single wafer processing, including the support thereof, especially in connection with relatively large diameter wafers (of about or more than 300 mm), and advantages thereof, as discussed previously.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

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To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 843.43178X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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